What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

first, second, and third wells being each of a second conductivity type opposite to said first conductivity type and provided in said semiconductor substrate;

a first field-effect transistor being of a first channel conductivity type and driven by a first supply voltage, and a second field-effect transistor driven by a second supply voltage larger in absolute value than said first supply voltage, the first and second transistors being arranged in said first well;

a third field-effect transistor being of said first channel conductivity type and driven by said first supply voltage, the third transistor being arranged in said second well;

a fourth field-effect transistor being of a first channel conductivity type and driven by said second supply voltage, the fourth transistor being arranged in said third well;

a first isolation layer provided between said first and second field-effect transistors; and

a second isolation layer provided between said first and second wells and between said second and third wells,

wherein said second supply voltage is supplied to said first well,

said first supply voltage is supplied to said second well,

said second supply voltage is supplied to said third well, and

said second isolation layer is wider than said first isolation layer.

2. The semiconductor device according to claim 1,

wherein a threshold voltage of said first field-effect transistor is set lower than that of said second field-effect transistor.

3. The semiconductor device according to claim 1,

wherein a gate insulator of said first field-effect transistor and that of said second field-effect transistor are equal to each other in thickness.

4. The semiconductor device according to claim 1,

wherein said second field-effect transistor is a field-effect transistor constituting a memory cell of an SRAM, and said first field-effect transistor is a field-effect transistor constituting a peripheral circuit of said SRAM.

5. The semiconductor device according to claim 4,

wherein said first, second, and third wells are provided so that they are respectively enclosed within first, second, and third buried wells, each of which is of said first conductivity type.

6. A semiconductor device comprising:

a semiconductor substrate of a first conductivity

type;

first, second, and third buried wells being each of a second conductivity type opposite to said first conductivity type and provided in said semiconductor substrate;

first, second, and third wells being each of a second conductivity type and provided so that they are respectively enclosed within said first, second, and third buried wells;

a first field-effect transistor being of said first channel conductivity type and driven by a first supply voltage, and a second field-effect transistor being of said first channel conductivity type and driven by a second supply voltage larger in absolute value than said first supply voltage, the first and second transistors being provided in said first well;

a third field-effect transistor being of said first channel conductivity type and driven by said first supply voltage, the third transistor being arranged in said second well;

a fourth field-effect transistor of said first channel conductivity type and driven by said second supply voltage, the fourth transistor being arranged in said third well;

a first isolation layer provided between said first and second field-effect transistors; and

a second isolation layer provided between said first

and second wells and between said second and third wells,

wherein said second supply voltage is supplied to said first well,

said first supply voltage is supplied to said second well,

said second supply voltage is supplied to said third well, and

said second isolation layer is wider than said first isolation layer.

7. The semiconductor device according to claim 6,

wherein a threshold voltage of said first field-effect transistor is set lower than that of said second field-effect transistor.

8. The semiconductor device according to claim 6,

wherein a gate insulator of said first field-effect transistor and that of said second field-effect transistor are equal to each other in thickness.

9. The semiconductor device according to claim 6,

wherein said second field-effect transistor is a field-effect transistor constituting a memory cell of an SRAM, and said first field-effect transistor is a field-effect transistor constituting a peripheral circuit of said SRAM.

10. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first buried well being of a second conductivity

type opposite to said first conductivity type and provided in said semiconductor substrate;

a first well being of said second conductivity type and provided so that the first well is enclosed within said first well;

a first field-effect transistor being of said first channel conductivity type and driven by a first supply voltage; and

a second field-effect transistor being of said first channel conductivity type and driven by a second supply voltage larger in absolute value than said first supply voltage,

wherein the first and second field-effect transistors are arranged in said first well, and

wherein said second supply voltage is supplied to said first well.

11. The semiconductor device according to claim 10, further comprising:

a fourth well of said first conductivity type is provided so that the fourth well is enclosed within said first buried well; and

a fifth field-effect transistor of said second channel conductivity type opposite to said first channel conductivity type is arranged in said fourth well.

12. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first buried well being of a second conductivity type opposite to said first conductivity type and provided in said semiconductor substrate;

fifth and sixth wells being each of said second conductivity type and provided so that they are enclosed within said first buried well;

seventh and eighth wells being each of said first conductivity type and provided so that they are enclosed within said first buried well;

a first field-effect transistor being of said first channel conductivity type and driven by a first supply voltage, the first transistor being arranged in said fifth well;

a second field-effect transistor being of said first channel conductivity type and driven by a second supply voltage larger in absolute value than said first supply voltage, the second transistor being arranged in said sixth well;

a sixth field-effect transistor being of said second channel conductivity type opposite to said first channel conductivity type, the sixth transistor being arranged in said seventh well; and

a seventh field-effect transistor of said second channel conductivity type, the seventh transistor being arranged in said eighth well,

wherein said second supply voltage is supplied to both said fifth and sixth wells.

13. The semiconductor device according to claim 12, further comprising:

second and third buried wells, each of said second conductivity type, provided in said semiconductor substrate;

a ninth well of said second conductivity type provided so that the ninth well is enclosed within said second buried well;

an eighth field-effect transistor of said first channel conductivity type, driven by said first supply voltage and arranged in said ninth well;

a tenth well of said second conductivity type provided so that the tenth well is enclosed within said third buried well;

a ninth field-effect transistor of said first channel conductivity type, driven by said second supply voltage and arranged in said tenth well;

a first isolation layer provided between said first and second field-effect transistors; and

a second isolation layer provided between said first and second wells and between said second and third wells,

wherein said second isolation layer is wider than said first isolation layer, and

wherein said first supply voltage is supplied to said ninth well, and said second supply voltage is supplied to said tenth well.

14. A semiconductor device, comprising:

a semiconductor substrate of a first conductivity type;

a first buried well being of a second conductivity type opposite to the first conductivity type and provided in said semiconductor substrate;

fifth and sixth wells being each of said second conductivity type and provided so that they are enclosed within said first buried well;

an eleventh well being of said first conductivity type and provided between said fifth and sixth wells so that the eleventh well is enclosed within said first buried well;

a first field-effect transistor being of said first channel conductivity type and driven by a first supply voltage, the first transistor being arranged in said fifth well;

a second field-effect transistor being of said first channel conductivity type and driven by a second supply voltage larger in absolute value than said first supply voltage, the second transistor being arranged in said sixth well; and

a sixth field-effect transistor of said second channel conductivity type opposite to said first channel conductivity type, the sixth transistor being arranged in said eleventh well,

wherein said second supply voltage is supplied to both of said fifth and sixth wells.

15. The semiconductor device according to claim 14, further comprising:

second and third buried wells being each of a second conductivity type are provided in said semiconductor substrate;

a twelfth well of said second conductivity type provided so that the twelfth well is enclosed within said second buried well;

an eighth field-effect transistor of said first channel conductivity type, driven by said first supply voltage and arranged in said twelfth well;

a thirteenth well is provided so that it is enclosed within said third buried well;

a ninth field-effect transistor of said first channel conductivity type, driven by said second supply voltage and arranged in said thirteenth well;

a first isolation layer provided between said first and second field-effect transistors; and

a second isolation layer provided between said first and second wells and between said second and third wells,

wherein said second isolation layer is wider than said first isolation layer, and

wherein said first supply voltage is supplied to said twelfth well, and said second supply voltage is supplied to said thirteenth well.